REMARKS

This Amendment is in response to the Office Action mailed 06/03/2004. In the Office Action, the Examiner rejected claims 1-20 under 35 U.S.C. § 102. Reconsideration in light of the remarks made herein is respectfully requested. No claims are amended

Rejection Under 35 U.S.C. § 102

2. The Examiner rejects claims 1-2, 4-5, 7-8, and 10-11 under 35 U.S.C. § 102(a) as being anticipated by Applicant's admitted prior art (US 2003/0074601 A1).

As per claim 1:

The Examiner asserts that Prior Art teaches "using processor implementation-specific instructions [col. 1, lines 53-56 [sic]] to save a processor state [col. 1 [0002], lines 11-15] in a system memory when a machine check error is generated by a processor [col. 1 [0002], lines 9-10]" and "attempting to correct the error [col. 1 [0002], lines 1-2] using processor implementation-specific instructions [col. 1 [0001], lines 7-10; and col. 1 [0002], lines 9-11]." Applicant respectfully disagrees.

In paragraph [0013] of the specification as filed applicant stated, "The term 'processor implementation-specific instructions' is used to mean a unit of one or more instructions that depend on the specific architecture or implementation of the processor to function correctly." Applicant finds nothing in the cited potion of Prior Art that discloses the use of processor implementation-specific instructions. In paragraph [0013] of the specification as filed applicant stated, "The term "processor-independent instructions" is used to mean a unit of one or more instructions that function correctly regardless of the specific architecture or implementation of the processor." Applicant respectfully submits that the disclosure of Prior Art only discloses the use of processor-independent instructions.

As per claim 2:

The Examiner asserts that Prior Art teaches "providing processor error record information obtained using processor implementation-specific instructions [col. 1 [0002], lines 2-4]." Applicant respectfully disagrees. Applicant finds nothing in the cited potion of Prior Art that discloses the use of processor implementation-specific instructions as defined by applicant's specification.

As per claim 4:

The Examiner asserts that Prior Art teaches "receiving control from processor-independent instructions indicates that the error has been corrected [col. 1 [0002], lines 2-4]." Applicant respectfully disagrees. Applicant finds nothing in the cited potion of Prior Art that discloses the use of processor implementation-specific instructions as defined by applicant's specification.

As per claim 5:

The Examiner asserts that Prior Art teaches "obtaining an address of a location to save the processor state in the system memory provided by platform-specific instructions [col. 1 [0002], lines 11-15]." Applicant respectfully disagrees. Applicant finds nothing in the cited potion of Prior Art that discloses the use of processor implementation-specific instructions as defined by applicant's specification.

As per claims 7-8 and 10-11:

The Examiner rejects claims 7-8 and 10-11 under the same rationale applied against claims 1-2 and 4-5. Applicant likewise traverses the rejection of claims 7-8 and 10-11 with the same rationale applied for claims 1-2 and 4-5.

Applicant respectfully requests that the Examiner withdraw the rejection of claims 1-2, 4-5, 7-8, and 10-11 under 35 U.S.C. § 102(a) as being anticipated by Prior Art.

3. The Examiner rejects claims 1-20 under 35 U.S.C. § 102(e) as being anticipated by Klecka et al. (US 6,393,582).

As per claim 1:

The Examiner asserts that Klecka teaches "using processor implementation-specific instructions [col. 1, lines 53-56] to save a processor state [abstract, col. 1, line 64] in a system memory when a machine check error is generated by a processor [abstract, col. 1, lines 5-10]" and "attempting to correct the error [col. 3, line 40] using processor implementation-specific instructions [col. 1, lines 62-64, col. 7, lines 59-64]." Applicant respectfully disagrees.

In paragraph [0013] of the specification as filed applicant stated, "The term 'processor implementation-specific instructions' is used to mean a unit of one or more instructions that depend on the specific architecture or implementation of the processor to function correctly." Applicant finds nothing in the cited potion of Klecka that discloses the use of processor implementation-specific instructions. In paragraph [0013] of the specification as filed applicant stated, "The term "processor-independent instructions" is used to mean a unit of one or more instructions that function correctly regardless of the specific architecture or implementation of the processor." Applicant respectfully submits that the disclosure of Klecka only discloses the use of processor-independent instructions.

As per claim 2:

The Examiner asserts that Klecka teaches "providing processor error record information obtained using processor implementation-specific instructions [col. 3, lines 29-44, col. 10, lines 53-58]." Applicant respectfully disagrees. Applicant finds nothing in the cited potion of Klecka that discloses the use of processor implementation-specific instructions as defined by applicant's specification.

As per claim 3:

Applicant relies on the patentability of the claims from which this claim depends to traverse the rejection without prejudice to any further basis for patentability of this claim based on the additional elements recited.

As per claim 4:

The Examiner asserts that Klecka teaches "receiving control from processor-independent instructions indicates that the error has been corrected [col. 2, lines 1-3]." Applicant respectfully disagrees. Applicant finds nothing in the cited potion of Klecka that discloses the use of processor implementation-specific instructions as defined by applicant's specification.

As per claim 5:

The Examiner asserts that Klecka teaches "obtaining an address of a location to save the processor state in the system memory provided by platform-specific instructions [col. 8, lines 61-67, and col. 8, lines 34-35]." Applicant respectfully disagrees. Applicant finds nothing in the cited potion of Klecka that discloses the use of processor implementation-specific instructions as defined by applicant's specification.

As per claim 6:

The Examiner asserts that Klecka teaches "attempting to correct the error using processor implementation-specific instructions is not done if an expected machine check indicator is set [col. 10, lines 50-57, and col. 13 [sic], lines 52-58]." Applicant has assumed that the Examiner intended to cite col. 12, lines 52-58, as there is no col. 13. Applicant respectfully disagrees with the Examiner's assertion. Applicant finds nothing in the cited potion of Klecka that discloses the use of an expected machine check indicator.

As per claims 7-13:

The Examiner rejects claims 7-13 under the same rationale applied against claims 1-6. Applicant likewise traverses the rejection of claims 7-13 with the same rationale applied for claims 1-6.

As per claims 14-20:

The Examiner rejects claims 14-20 under the same rationale applied against claims 1-6. Applicant likewise traverses the rejection of claims 14-20 with the same rationale applied for claims 1-6.

Applicant respectfully requests that the Examiner withdraw the rejection of claims 1-20 under 35 U.S.C. § 102(e) as being anticipated by Klecka.

Conclusion

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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Dated: August 16, 2004 By

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